



Attorney's Docket No. 42P18257

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:)
Nick Lindert et al.) Examiner: Nguyen, Joseph H.
Application No.: 10/816,311) Art Unit: 2815
Filed: March 31, 2004)
For: BULK NON-PLANAR TRANSISTOR)
HAVING STRAINED ENHANCED)
MOBILITY AND METHODS OF)
FABRICATION)

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

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Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

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- 1 -

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X 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 7/11, 2005

m a e c e e s

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

JUL 13 2005

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	us-	20040031979 A1	02/19/2004	Lochtefeld et al.	
	us-	6,716,684 B1	4/6/2004	Krivokapic et al.	
	us-	6,680,240 B1	1/20/2004	Maszara	
	us-	6,562,665 B1	5/13/2003	Yu	
	us-	6,525,403 B2	2/25/2003	Inaba et al.	
	us-	6,475,869 B1	11/5/2002	Yu	
	us-	5,563,077	10/8/1996	Ha	
	us-	5,346,839	9/13/1994	Sundaresan	
	us-	2002/0081794 A1	6/27/2002	Ito	
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	us-	5,658,806	8/19/1997	Lin et al.	
	us-	6,376,317 B1	4/23/2002	Forbes et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
		EP 0 623 963 A1	11/9/1994	Siemens AG		
		WO 02/43151A	5/30/2002	Hitachi ULSI Sys Co Ltd		

Examiner Signature

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language translation is attached.

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Attorney Docket Number

Complete if Known

Application Number	10/816,311
Filing Date	3/31/2003
First Named Inventor:	Nick Lindert
Art Unit	2815
Examiner Name	Nguyen, Joseph

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		T. Park et al., "Fabrication of Body-Tied FinFETs (Omega MOSFETS) Using Bulk Si Wafers", 2003 Symposia on VLSI Technology Digest of Technical Papers, June 2003, pages 135-136.	
		V. Subramanian et al., " A Bulk-Si-Compatible Ultrathin-body SOI Technology for Sub-100m MOSFETS" Proceeding of the 57th Annual Device Research Conference, pp. 28-29 (1999)	
		Hisamoto et al., "A Folded-channel MOSFET for Deepsub-tenth Micron Era", 1998 IEEE International Electron Device Meeting Technical Digest, pp 1032-1034 (1998)	
		Huang et al., "Sub 50-nm FinFET: PMOS", 1999 IEEE International Electron Device Meeting Technical Digest, pp 67-70 (1999)	
		Auth et al., "Vertical, Fully-Depleted, Surroundings Gate MOSFETS On sub-0.1um Thick Silicon Pillars", 1996 54th Annual Device Research Conference Digest, pp 108-109 (1996)	
		Hisamoto et al., "A Fully Depleted Lean-Channel Transistor (DELTA)-A Novel Vertical Ultrathin SOI MOSFET", IEEE Electron Device Letters, V. 11(1), pp36-38 (1990).	
		Jong-Tae Park et al., "Pi-Gate SOI MOSFET" IEEE Electron Device Letters, Vol. 22, No. 8, August 2001, pages 405-406	
		Hisamoto, Digh et al. "FinFET- A Self-Aligned Double-Gate MOSFET Scalable to 20 nm", IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325	
		International Search Report PCT/US 03/26242	
		International Search Report PCT/US 03/39727	
		International Search Report PCT/US 03/40320	

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